UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,853	11/25/2003	Don T. Lam	1020.P16533	8556

57035 7590 03/20/2007

KACVINSKY LLC
C/O INTELLEVATE
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,853	LAM, DON T.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/06/2006 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-8, 10-11 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Amicangioli et al. (U.S. Pat. No. 6,327,242)

With respect to claims 1 and 15-16 Amicangioli teaches an isolation circuit, comprising: a control circuit (item 16 Fig. 1) to receive as input a power status signal (logic detects for power failure) and a software event signal (time out see col. 4 lines 55-

56), said control circuit (16) to output a switch control signal (switch modes from operational to standby), said switch control signal to comprise a switch close signal (position A switch is closed and operational) if said power status is valid, and a switch open signal (position B switch is open and in standby mode) if said power status is invalid, wherein an invalid power indicates detection of a power status interruption from the main line power supply; and at least one switch (item 14) to connect to said control circuit, said switch to receive said switch control signal and a component signal (LAN signals) and operate in accordance with said switch control signal, with said switch to prevent communication of said component signal when said switch is in an open state.

With respect to claim 2 Amicangioli teaches said control circuit outputs said control signal in accordance with said software event signal (i.e. expiry of watchdog timer).

With respect to claim 3 Amicangioli teaches said switch receives as input a software control signal (explicit signals passed via line 19), and said switch switches between said open state and a closed state in accordance with said software control signal.

With respect to claim 4 Amicangioli teaches a plurality of switches (items 14-1 and 14-2), each switch to connect to said control circuit (16), said plurality of switches to each receive said switch control signal (see dashed lines in Fig. 1) and a component signal (LAN or WAN signals) and operate in accordance with said switch control signal, with said plurality of switches to prevent communication of said component signals when said switch is in an open state (standby mode).

With respect to claim 7 Amicangioli teaches a system, comprising: a bus (network item 15); a shelf (item 30) having a plurality of shelf components (item 20 and 30); a management module (item 10) to connect to said bus (15), said management module (10) to manage a plurality of signals (network communications signals) communicated between said shelf components; and wherein said management module comprises an isolation circuit (item 14) to isolate said shelf component signals upon detection of a power interruption (see col. 4 lines 55-56) from one or more power supplies (not shown) to one of said shelf components.

With respect to claim 8 Amicangioli teaches isolation circuit comprises: a control circuit (item 16) to receive as input a power status signal (logic detects for power failure see col. 4 lines 55-56), said control circuit (16) to output a control signal (shown by dashed lines in Fig. 1), said control signal to comprise a switch close signal (normal operation signal i.e. switch position "A") if said power status is valid, and a switch open signal if said power status is invalid (standby operation signal i.e. switch position "B"); and at least one switch (item 14) to connect to said control circuit (16), said switch to receive said control signal and at least one of said shelf component signals (network communication signal) and operate in accordance with said control signal, with said switch to prevent communication of said shelf component signal when said switch is in an open state (standby state).

With respect to claim 10 Amicangioli teaches said control circuit receives as input a software event signal (time out see col. 4 lines 55-56), and said control circuit outputs

said control signal in accordance with said software event signal (switch to standby mode after expiry of timer).

With respect to claim 11 Amicangioli teaches said switch receives as input a software control signal (shown as dashed lines in Fig. 1), and said switch switches (item 14) between said open state (operational mode) and a closed state (standby mode) in accordance with said software control signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amicangioli et al. (U.S. Pat. No. 6,327,242) in view of Edelen et al. (U.S. Pat. No. 6,789,871)

With respect to claim 5 Amicangioli teaches control circuit (16) receives power from a power supply (not shown), and when said control circuit fails (col. 4 lines 55-56) to receive said power said control circuit drives said switch to an open state (standby mode). Amicangioli does not clearly depict the power supply or describe its connection is the system, however one of ordinary skill would understand the connection of a power

supply to the server (items 20 or 30) to power the system a required and necessary component to enable operation of the system.

With respect to claim 6 Amicangioli teaches the control circuit and control logic merely as block diagrams and does not describe in detail the types of circuitry utilized in the implementation, It would have been obvious to one of ordinary skill in the art at the time of the invention to use n-channel MOSFET as the use of such solid state circuitry in control logic is commonly implemented in digital switching logic for its low loss and high speed switching characteristics. Edelen also teaches a plurality of switches which are configured to receive a component signal; a control circuit item 340 couple to said plurality of switches and also provides the teaching of dual channel MOSFETs are an obvious substitute for FET relays or other type of switch

Claims 9 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amicangioli et al. (U.S. Pat. No. 6,327,242)

With respect to claim 9 Amicangioli teaches said control circuit receives power from a power supply (not shown), and when said control circuit fails to receive said power said control circuit drives said switch to an open state (logic detects for power failure and transitions to standby state see col. 4 lines 55-56). Amicangioli does not clearly depict the power supply or describe its connection is the system, however one of ordinary skill would understand the connection of a power supply to the server (items 20 or 30) to power the system a required and necessary component to enable operation of the system.

With respect to claims 17 and18 Amicangioli teaches said closing and opening comprises: receiving said power status signal indicating power is valid; and sending current to close and open said switch. Amicangioli dose not describe the closing a TTL type signal. The use of transistor logic signals is well known in the switching logic circuits such as that of Amicangioli. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a transistor logic signal if in fact this is not operation of Amicangioli in order to utilize the advantages of transistors and solid-state devices.

With respect to claims 19 and 20 Amicangioli teaches said isolating comprises: receiving a software event signal from an application program (watchdog timer) at said control circuit (16) and switch; and opening said switch to prevent said component signal from being communicated to an external module (modules connected to LAN for example NIC item 22) in accordance with said software event signal.

Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over in Amicangioli et al. (U.S. Pat. No. 6,327,242) in view of Gill et al. (U.S. Pat. No. 5,388,032)

With respect to claim 12 Amicangioli teaches a plurality of switches (item 14-1 and 14-2), each switch to connect to said control circuit (item 16) to electrically couple to said plurality of switches. Amicangioli does not teach the detailed transistor level logic used in the logic circuitry. MOSFET and transistor solid-state devices are commonly utilized in switching circuitry due to small power required and low losses involved in MOSFET or CMOS transistor logic. Gill teaches a network and monitor type device and

discriminator controller (item 194) similar to the controller of Amicangioli. Gill further teaches standard implementation of a dual channel n-mos device (col. 25 lines 68 – col. 26 lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to use standard dual N-channel MOSFET transistor logic such that a first and second MOSFET connected within the control logic circuitry in order to output the appropriate transistor logic signal to each switch in order to isolate the component signals when a power failure or software event has occurred within the system.

With respect to claim 13 Gill teaches the logic of an open switch when the power is removed (power is false). Amicangioli teaches the logic is also open when the power has failed

With respect to claim 14 Amicangioli as modified by Gill render obvious the limitation the control signal is sent to the switch by a software control signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800